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(54) **FEEDBACK IMPEDANCE CONTROL FOR DRIVING A SIGNAL**

(71) Applicant: **Broadcom Europe Limited**, London (GB)

(72) Inventor: **Jonathan Ephraim David Hurwitz**, Edinburgh (GB)

(73) Assignee: **Broadcom Europe Limited**, London (GB)

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This patent is subject to a terminal disclaimer.

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Related U.S. Application Data

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H04M 1/00 (2006.01)
H04B 3/54 (2006.01)

(52) **U.S. Cl.**
CPC **H04B 3/542** (2013.01); **H04B 3/54** (2013.01); **H04B 2203/5425** (2013.01)

(58) **Field of Classification Search**
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2203/5483; H04B 2203/5491; H04B 2203/5495; H04B 2203/5408; H04B 2203/5466; H04B 2203/542; H04B 1/69; H04B 1/07; G01R 31/31924; G01R 31/3183; G01R 31/318307; G01R 31/319; G01R 31/31908; G01R 17/02; G01R 19/0053; G01R 31/02; H04Q 1/46; H04M 11/002; H04M 9/001; H04M 9/10; H04M 1/76; H04M 11/062
USPC 379/30, 93.36, 102.04, 106.04, 322, 379/386, 388.03, 388.05, 388.07, 390, 379/390.01, 390.03, 394, 395, 395.01, 398, 379/399.01, 106.03, 167.01, 171, 93.01; 381/120, 121

See application file for complete search history.

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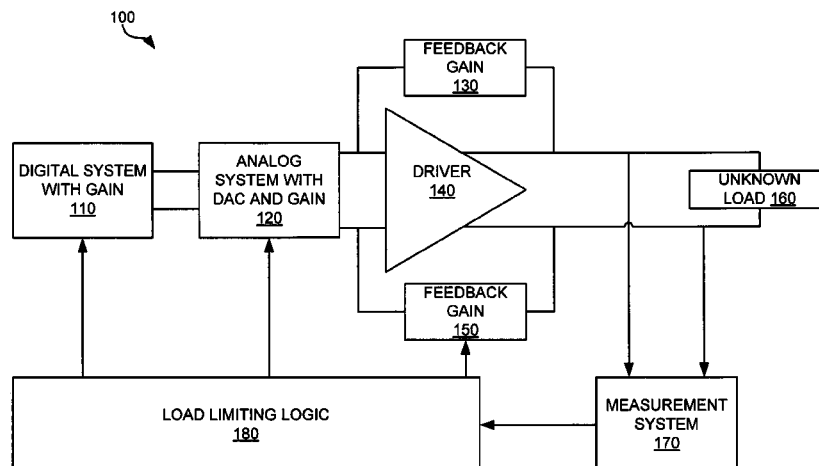
Primary Examiner — Akelaw Teshale

(74) *Attorney, Agent, or Firm* — Garlick & Markison; Randy Lacasse

(57) **ABSTRACT**

A system for driving a first signal onto a wireline includes a driver and feedback circuitry. The driver drives a deterministic signal onto the wireline with an unknown impedance load. The feedback circuitry measures a quality of the output signal from the wireline and modifies a gain of the first signal based on the quality of the output signal. The driver then drives the first signal onto the wireline with the modified gain.

20 Claims, 6 Drawing Sheets



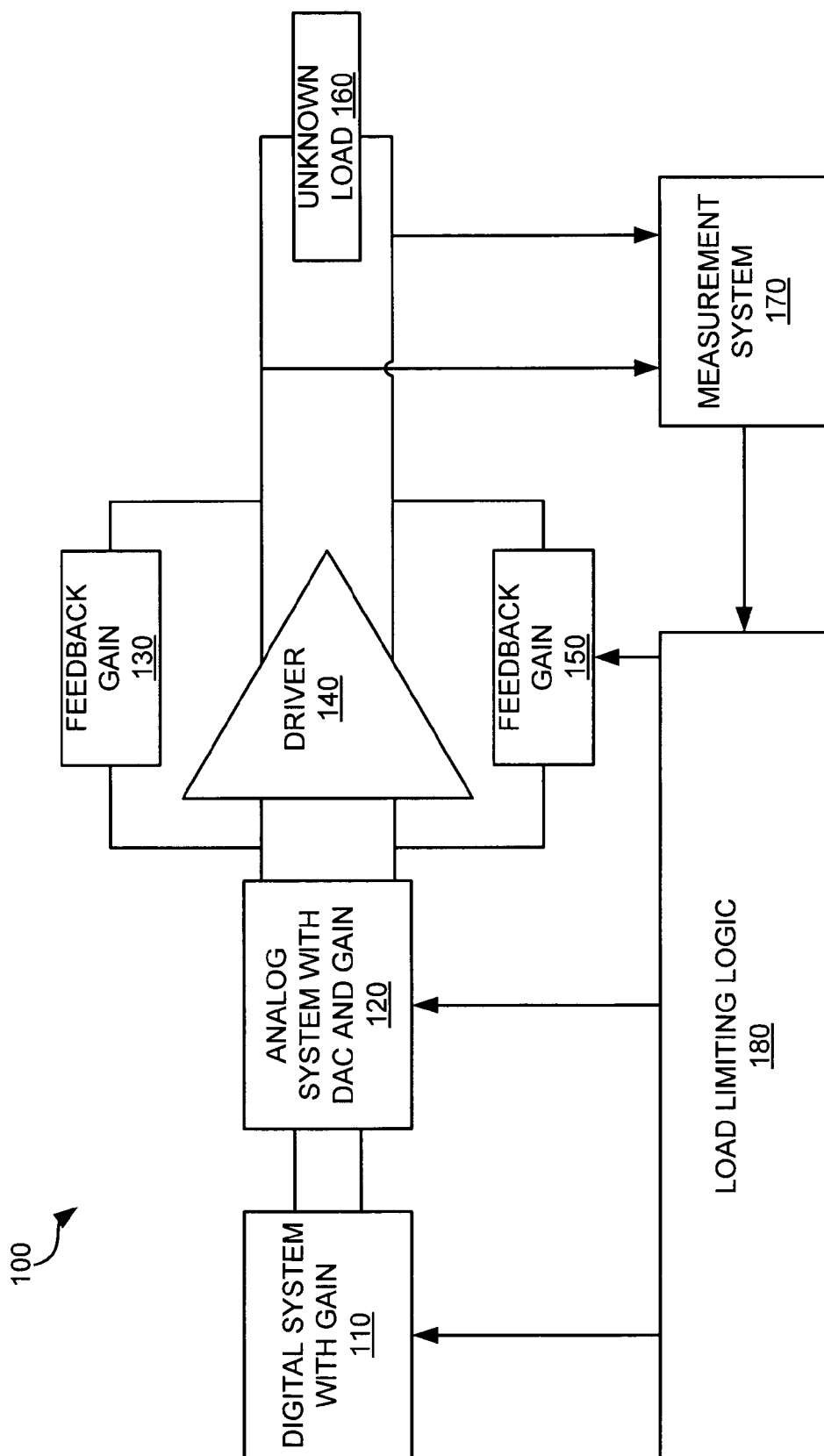


FIG. 1

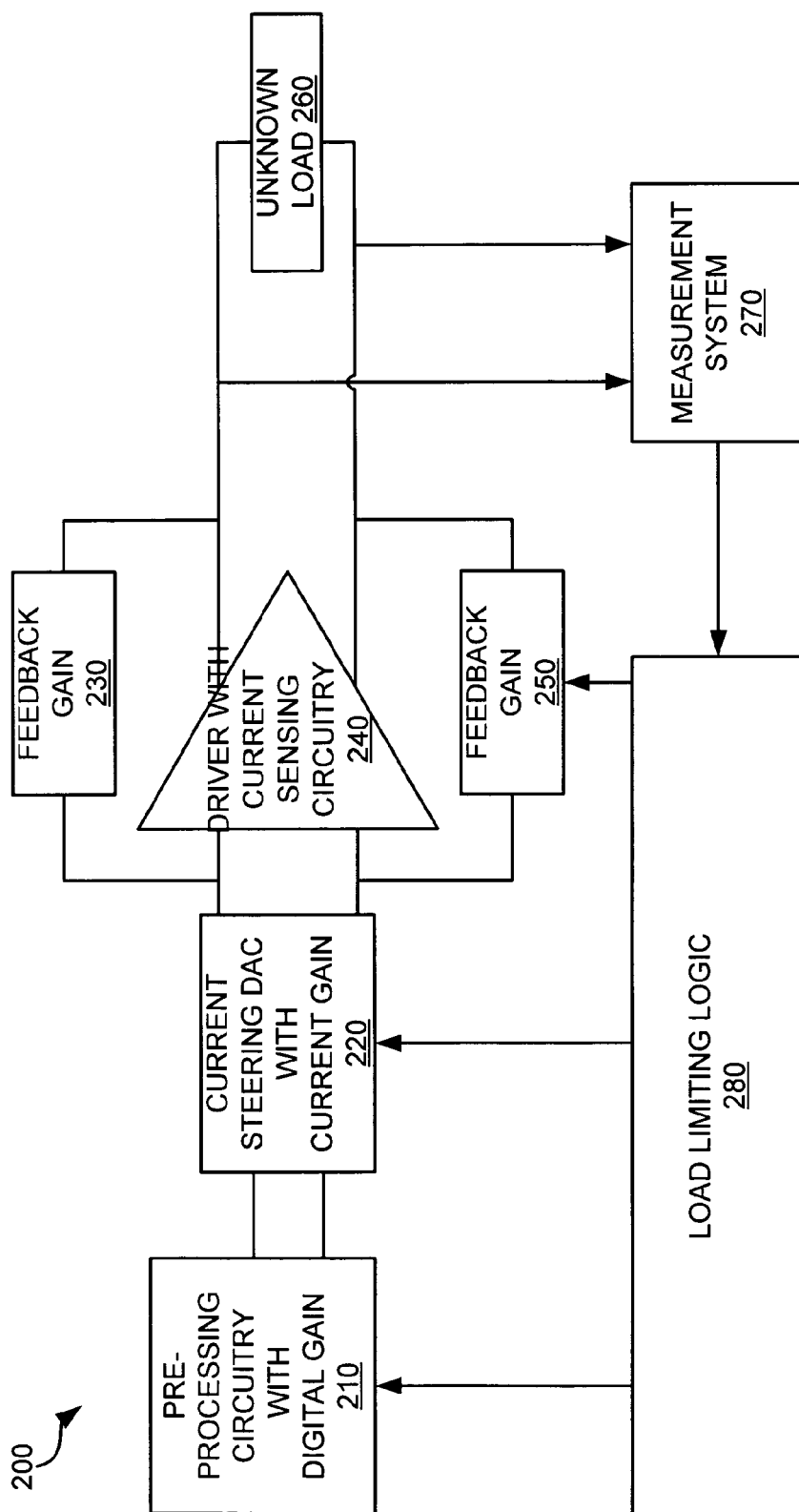


FIG. 2

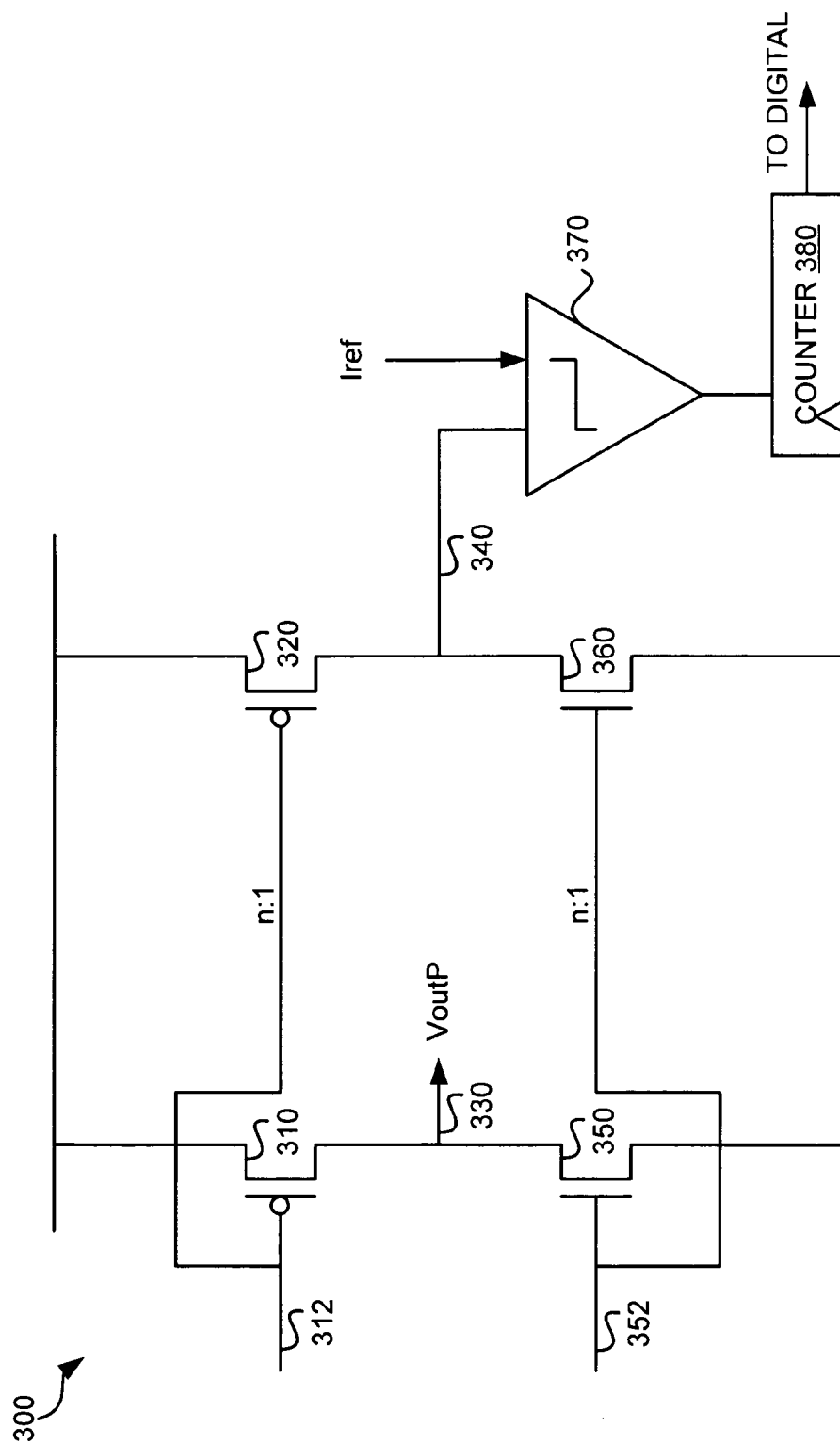


FIG. 3

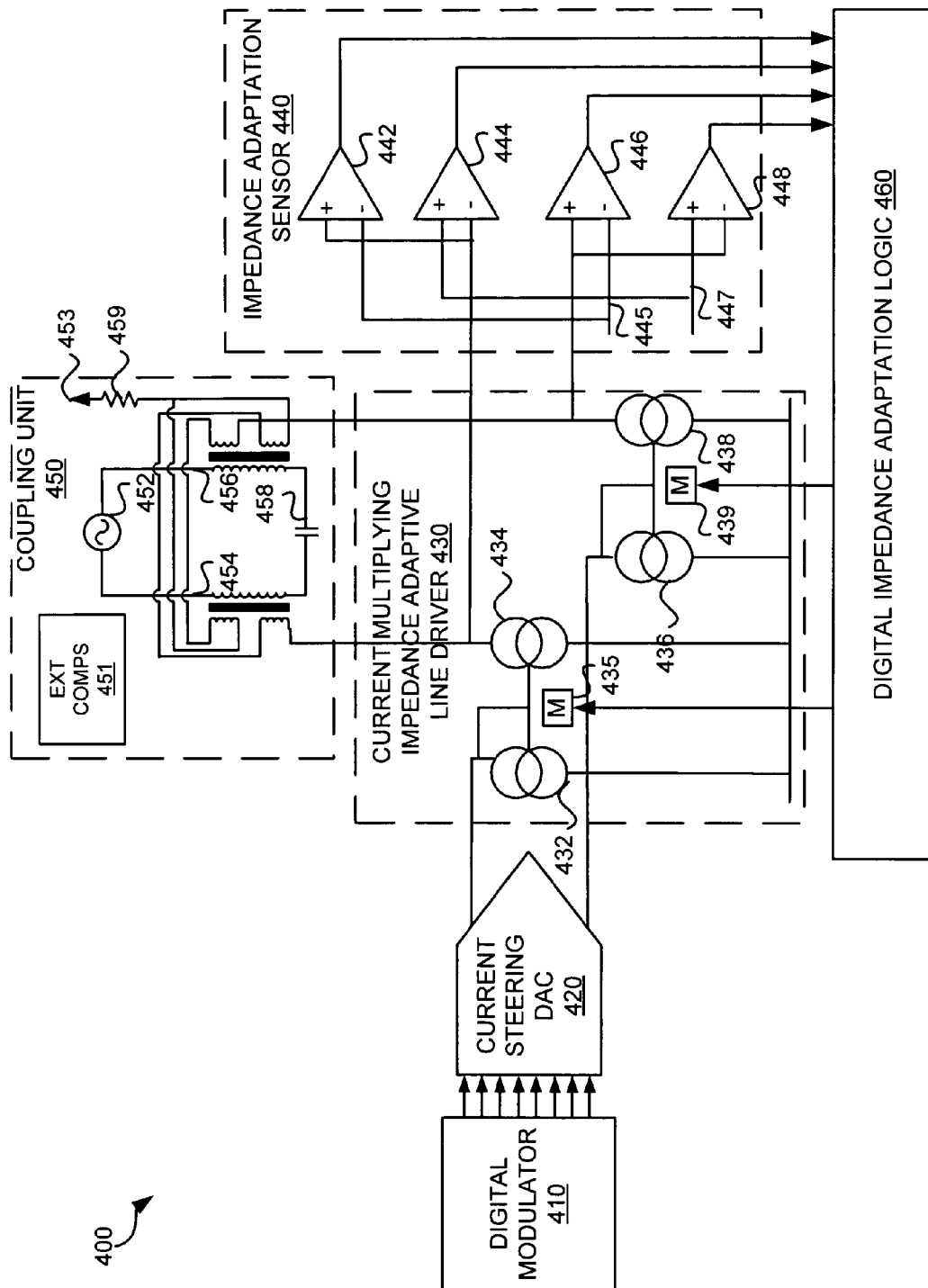


FIG. 4

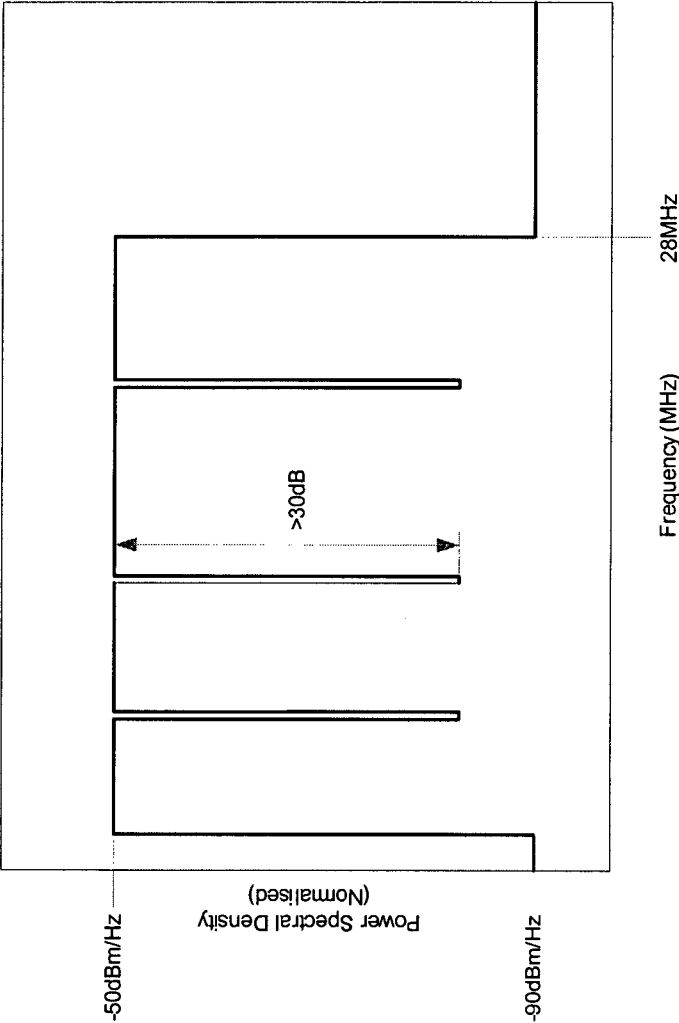


FIG. 5

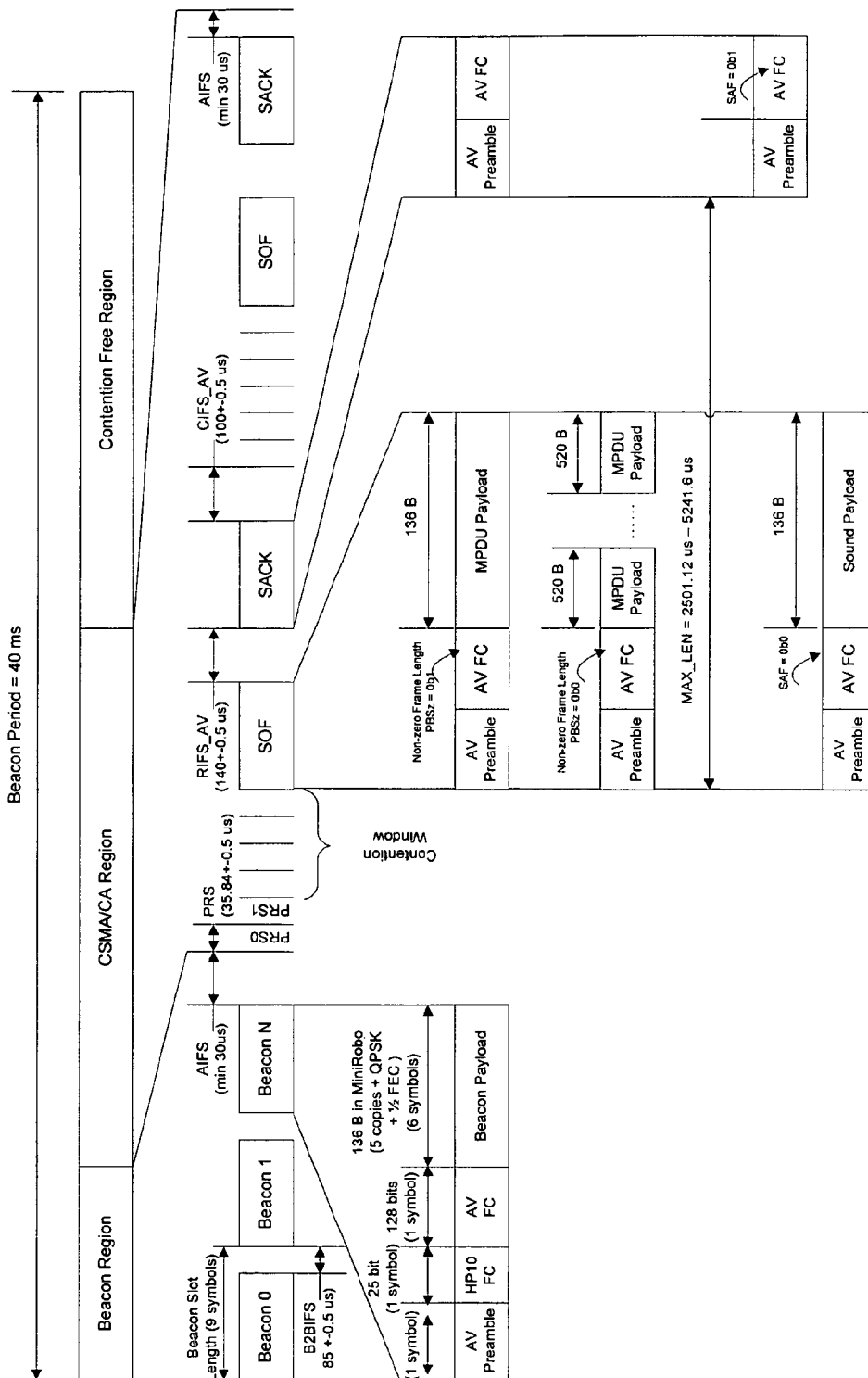


FIG. 6

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FEEDBACK IMPEDANCE CONTROL FOR DRIVING A SIGNAL

CROSS REFERENCE TO RELATED PATENTS

The present U.S. Utility Patent Application claims priority pursuant to 35 U.S.C. §120 as a continuation of U.S. Utility application Ser. No. 11/493,292 entitled "Feedback Impedance Control for Driving a Signal", filed Jul. 25, 2006, which is hereby incorporated herein by reference in its entirety and made part of the present U.S. Utility Patent Application for all purpose.

STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR DEVELOPMENT

Not Applicable

INCORPORATION-BY-REFERENCE OF MATERIAL SUBMITTED ON A COMPACT DISC

Not Applicable

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention relates generally to driving a signal on a wireline and more particularly to feedback impedance control for driving a signal.

2. Description of Related Art

A line driver drives a signal that is suitable for transmission over a wired connection. The difficulty of driving a signal onto a wired connection increases when the impedance on the wired connection is unknown and dynamic. One example of wired connections is a powerline network used for communications such as a residential powerline.

One limitation with powerline is that the impedance of the network can be unknown. There are regulations and standards that specify emission and performance requirements for a device connected to the powerline for a known impedance such as 50 ohms. However, the actual impedance of powerline can have a wide range such as from 5 ohms to 300 ohms, both from one node to another node and within the frequency range utilized in the communications system. The impedance has a wide range because the impedance depends on the network topologies (e.g. star and ring), the wiring, the connections, and the devices or appliances plugged into the sockets of the powerline with the effects of reflections combining with the passive characteristics to make a complex impedance. Furthermore, the impedance of the powerline can be dynamic (i.e. change during operation). For example, a timer may turn on a heater, which significantly increases the load upon the powerline.

Another limitation is that the impedance changes with frequency. In a band of 2 MHz to 30 MHz, the impedance is different at 2 MHz than at 30 MHz. Plus, the impedances at the different frequencies behave like a complex load as opposed to a simple load such as a resistor.

Some wired communications systems use complex multi-carrier modulation schemes that put particular requirements on inter-carrier modulation interference to achieve performance or even pass regulations. In powerline, high density orthogonal frequency division multiplexing (OFDM) typically uses a large number of carriers such as greater than 200. The non-linearity in the line driver may cause interference, which can degrade the performance of the wireline (e.g.

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degrading signal-to-noise ratio in other carriers). This non-linearity in the line driver may cause problems for other modulation schemes.

A line driver can use two different basic drive schemes: voltage buffering and current steering, voltage buffering being the more common. The challenge with voltage buffering is to prevent distortion by trying to drive too much current for the design when the impedance is low. The challenge with current steering is to prevent distortion by generating too much voltage than was designed for when resistance is high.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is an illustration of a system for driving a signal in an exemplary implementation of the invention.

FIG. 2 is an illustration of a system for driving a signal with a voltage drive in an exemplary implementation of the invention.

FIG. 3 is an illustration of current sensing circuitry in an exemplary implementation of the invention.

FIG. 4 is an illustration of a system with a current multiplying digital to analog converter and a comparator in an exemplary implementation of the invention.

FIG. 5 is a graph of frequency (in MHz) vs. power spectral density (normalized).

FIG. 6 is an illustration of data frame of a beacon period in an exemplary implementation of the invention.

DETAILED DESCRIPTION OF THE INVENTION

The embodiments discussed herein are illustrative of one example of the present invention. As these embodiments of the present invention are described with reference to illustrations, various modifications or adaptations of the methods and/or specific structures described may become apparent to those skilled in the art. All such modifications, adaptations, or variations that rely upon the teachings of the present invention, and through which these teachings have advanced the art, are considered to be within the scope of the present invention. Hence, these descriptions and drawings should not be considered in a limiting sense, as it is understood that the present invention is in no way limited to only the embodiments illustrated.

A system for driving a first signal onto a wireline includes a driver and feedback circuitry. The driver drives a deterministic signal onto the wireline with an unknown impedance load. The feedback circuitry measures a quality of an output signal from the wireline and modifies a signal strength of the first signal based on the quality of the output signal. The driver then drives the first signal onto the wireline.

By providing feedback impedance control for driving a signal, the system advantageously can handle worst case scenarios when impedance is low or high. The system can also reduce power consumption by efficiently driving the signal onto the wireline. The system can also meet standards or requirements for qualification loads and reduce distortion and inter-carrier interference. The system can also prevent signal degradation as the impedance changes during operation. The system may also be applied to different types of drive schemes such as voltage buffering and current steering. The system may also be used in low-voltage CMOS, where voltage and current may be limited.

FIG. 1 depicts an illustration of a system 100 for driving a signal in an exemplary implementation of the invention. The system 100 includes a digital system 110, an analog system with a digital to analog converter (DAC) 120, feedback gain

130, driver 140, feedback gain 150, an unknown load 160, a measurement system 170, and load limiting logic 180.

The digital system 110 is coupled to the analog system 120. The analog system 120 is coupled to the feedback gains 130 and 150 and the input of the driver 140. The output of the driver 140 is coupled to the feedback gain 130 and 150, the unknown load 160, and the measurement system 170. The measurement system 170 is coupled to the load limiting logic 180. The load limiting logic 180 is coupled to the digital system 110, the analog system 120, and the feedback gain 150.

The digital system 110 is any digital circuitry with gain. The digital system 110 may generate a deterministic signal. A deterministic signal is any test or known signal. Some examples of a deterministic signal are a test waveform, a known waveform (e.g. the preamble already in the communications and within the first signal), and a probabilistically known signal (e.g. data of the first signal). The analog system 120 is any analog circuitry with gain. In this embodiment, the analog system 120 includes a DAC.

The driver 140 is any circuitry configured to drive a signal onto a wireline. The driver 140 may be a high frequency line driver. In some embodiments, the wireline comprises a powerline. The frequency range in the powerline may be 2-30 MHz. Another frequency range may be 50-300 MHz. The powerline may use an OFDM modulation scheme. The powerline may also use adaptive multi-carrier code division multiple access, which is disclosed in U.S. patent application Ser. No. 11/482,373 entitled "Adaptive Multi-carrier Code Division Multiple Access" filed on Jul. 6, 2006, which is hereby incorporated by reference.

The feedback gain 130 and 150 are any circuitry that feeds the output of the driver 140 back into the input of the driver 140.

The unknown load 160 is any device or circuitry attached to the wireline that has an impedance that is unknown. The unknown load 160 may comprise speakers or other home entertainment equipment attached to a residential powerline. The unknown load 160 may also include other devices such as lights and appliances that plug into the residential powerline. In one example, the unknown load 160 could be between 5 ohms and 300 ohms.

The measurement system 170 is any circuitry or system configured to measure the quality of an output signal from the wireline. The measurement system 170 may measure current, voltage, distortion, signal-to-noise ratio, and/or heat. One measure of quality of the output signal is the distortion, which may be measured by signal-to-noise ratio by using a Fast Fourier Transform to determine signal content in the notches. The measurement system 170 may also directly or indirectly measure the operating point of the driver 140 such as the peak or average output current through a replica output stage. Also, an indirect measurement of the operating point may be temperature or voltage drop. In various embodiments, one or more measurements can be made to determine the quality of the signal.

The measurement and modification can occur continuously until the desired quality of the output signal is reached. The measurement and the following modification of the signal strength can occur at different times. The measurement and modification of the signal strength can occur on power-up or there can be a periodic measurement and modification (e.g. every few seconds). The measurement and modification can also be embedded in the normal communication system.

The load limiting logic 180 is any circuitry configured to modify the signal strength/swing of the signal. The load limiting logic 180 may modify the signal strength by changing

the gain. The signal may be changed by changing the signal swing by scaling the signal. For example, when the impedance is 50 ohms, 4 volts is driven peak-to-peak. Above 50 ohms, 4 volts will continue to be driven peak-to-peak. When the impedance is 25 ohms, the measurement system 170 determines that a condition occurred such as too much current is being used or too much distortion based on the measured quality of the output signal. The load limiting logic 180 then changes the signal so that 2 volts is driven peak-to-peak until the desired quality is achieved. Thus, less signal is injected but the signal is still within the operating range of the driver 140. Thus, the signal strength is changed but still matches the capabilities of the driver 140.

The load limiting logic 180 may be a processor or circuitry executing software or firmware. The load limiting logic 180 may use state machines or real time calculations. The load limiting logic 180 could operate continuously or be decision based. The load limiting logic 180 may change the R_{gain} of the digital system 110, the analog system 120, and the feedback gain 150 based on the current sensed. The gain may be changed in any circuitry that has input and outputs that are analog, digital, or a combination of analog and digital. Furthermore, the load limiting logic 180 that controls the gain change is digital but may also be an analog control system. The load limiting logic 180 may also change a multiplier or a DAC range setting, which could be greater than 4 bits.

The measurement system 170 and the load limiting logic 180 may be combined into a single feedback circuitry. The feedback circuitry is any circuitry configured to measure a quality of an output signal from the wireline and modify a signal strength of the first signal based on the quality of the output signal.

FIG. 2 depicts an illustration of a system 200 for driving a signal with a voltage drive in an exemplary implementation of the invention. The system 200 includes a digital pre-processing circuitry 210, a current steering DAC 220, feedback gain 230, driver 240 with current sensing circuitry 240, feedback gain 250, an unknown load 260, a measurement system 270, and load limiting logic 280.

The pre-processing circuitry 210 is coupled to the current steering DAC 220. The current steering DAC 220 is coupled to the feedback gains 230 and 250 and the input of the driver 240. The output of the driver 240 is coupled to the feedback gain 230 and 250, the unknown load 260, and the measurement system 270. The measurement system 270 is coupled to the load limiting logic 280. The load limiting logic 280 is coupled to the pre-processing circuitry 210, the current steering DAC 220, and the feedback gain 250.

The pre-processing circuitry 210 has digital gain. The current steering DAC has current gain. The driver 240 includes current sensing circuitry in the output stage, which is described in further detail in FIG. 3.

FIG. 3 depicts an illustration of current sensing circuitry 300 in an exemplary implementation of the invention. The current sensing circuitry 300 is located in the output stage of the driver 240 of FIG. 2. The current sensing circuitry 300 measures the current in the output stage of the driver 240 to determine the operating point of the driver 240. The output stage of the driver 240 is in a push-pull configuration.

The current sensing circuitry 300 comprises a PMOS transistor 310, a PMOS transistor 320, an NMOS transistor 350, an NMOS transistor 360, a comparator 370, and a counter 380. The sources of the PMOS transistors 310 and 320 are coupled to the source voltage. The gates of the PMOS transistors 310 and 320 are coupled to the input 312. The drains of the PMOS transistor 310 and the NMOS transistor 350 are coupled to the output VoutP 330. The gates of the NMOS

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transistors 350 and 360 are coupled to the input 352. The sources of the NMOS transistors 350 and 360 are coupled to ground. The drains of the PMOS transistor 320 and the NMOS transistor 360 are coupled to the input of the comparator 370. The output stage is formed from the PMOS transistor 310 and the NMOS transistor 350. The output stage is mirrored by the PMOS transistor 320 and the NMOS transistor 360. This mirror may operate at 100 times less current or some value n time less current than the output stage.

The other input of the comparator 370 is coupled to a link with a reference current, I_{ref} . The comparator 270 compares the reference current and the output signal from the output stage. The output of the comparator 370 is coupled to the counter 380. The counter 380 counts the number of times the output signal from the output stage goes beyond the reference current. The output of the counter 380 is coupled to a digital output.

FIG. 4 depicts an illustration of a system 400 with a current multiplying DAC and a comparator in an exemplary implementation of the invention. The system 400 comprises a digital modulator 410, a current steering DAC 420, a current multiplying impedance adaptive line driver 430, an impedance adaptation sensor 440, a coupling unit 450, and digital impedance adaptation logic 460. The digital modulator 410 is coupled to the current steering DAC 420.

The current multiplying impedance adaptive line driver 430 includes a transformer 432, a transformer 434, a multiplier 435, a transformer 436, a transformer 438, and a multiplier 439. The transformer 432, the transformer 434, and the multiplier 435 form a current mirror with a multiplier. The transformer 436, the transformer 438, and the multiplier 439 also form a current mirror with a multiplier. The current steering DAC 420 is coupled to the transformers 432, 434, and 436. The multipliers 435 and 439 are coupled to the digital impedance adaptation logic 460.

The coupling unit 450 includes external components 451, an AC power line 452, an analog V_{DD} output 453, a transformer 454, a transformer 456, a coupling capacitor 458, and a DC biasing resistor 459. In this example, the coupling unit 450 couples to the powerline network. The coupling unit 450 refers the impedance from the powerline in the form of capacitance or inductance. In some embodiments, the transformer 454 and 456 may form a 2000V isolation high frequency signal transformer. The AC power line 452 and the coupling capacitor 458 are coupled to the transformers 454 and 456. One example of the coupling capacitor 458 is the Y1 class low filter bypass capacitor. The resistor 459 is coupled to the transformer 456. The resistor 459 can also be coupled to the analog V_{DD} .

The impedance adaptation sensor 440 includes comparators 442, 444, 446, and 448. The outputs of the comparators 442, 444, 446, and 448 are coupled to the digital impedance adaptation logic 460. The impedance adaptation sensor 440 senses whether the voltage is above or below a threshold. The impedance adaptation sensor 440 determines some of the voltage swing characteristics. For example, with the negative input of the comparator 446 coupled to an underdrive reference link 445 and the negative input of the comparator 448 coupled to a clipping reference link 447, the amount of time the signal spends between the underdrive voltage and the clipping reference can be determined. The impedance adaptation sensor 440 shown in FIG. 4 is really a type of analog to digital converter and may be replaced by one that may already be in the system, such as on the receiver path.

The system 400 employs a current buffer. In one example, the impedance of the powerline is 100 ohms. The current is 10 milliamps. The peak-to-peak is then 1 volt. If the impedance

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is 200 ohms and the current is 10 milliamps, the peak-to-peak is 2 volts. The digital impedance adaptation logic 460 can then detect there is too much voltage and change the multiplication factors in the multipliers 435 and 439 to change the current to 5 milliamps to make the peak-to-peak voltage 1 volt.

FIG. 5 depicts a graph of frequency (in MHz) vs. power spectral density (normalized). This graph is an example of a standard requirement for power spectral density for powerline communications. The graph shows that there may be requirements to be 30 dB down or 40 dB down based on frequency. When distortion occurs, the frequencies are distorted from harmonics from adjacent frequencies would help fill in the notches.

FIG. 6 depicts an illustration of data frame of a beacon period in an exemplary implementation of the invention. The measurement of the deterministic signal could use parts of the data frame that is known. The measurement system 170 can measure characteristics of signals and perform a frame by frame comparison. If there is a change in the quality of the signal, the signal strength can then be modified.

The above description is illustrative and not restrictive. Many variations of the invention will become apparent to those of skill in the art upon review of this disclosure. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A system, comprising:

a transmission circuitry driver configured to drive a deterministic signal and a first signal onto a powerline in a powerline communication network with an unknown impedance load;

a digital system coupled to an input of the transmission circuitry driver and configured to produce the deterministic signal and the first signal;

feedback circuitry configured to measure a quality of an output signal from the powerline based on the deterministic signal and to modify a gain of the first signal produced by the digital system based on the quality of the output signal; and

wherein the first signal, with modified gain, is driven by the transmission circuitry driver onto the powerline.

2. The system of claim 1, wherein the feedback circuitry is configured to modify the gain of the first signal by changing a gain of the first signal in an analog system disposed between the digital system and the input of the transmission circuitry driver.

3. The system of claim 1, wherein the feedback circuitry is configured to modify the gain of the first signal by changing a gain of the first signal in a converter that converts between analog and digital.

4. The system of claim 1, wherein the feedback circuitry is configured to measure the quality of the output signal from the powerline and modify the gain of the first signal based on the quality of the output signal until a desired performance of the first signal is achieved.

5. The system of claim 1, wherein the feedback circuitry is configured to measure the quality of the output signal by measuring a distortion of the output signal, a voltage of the output signal or a current of the output signal.

6. The system of claim 1, wherein the deterministic signal comprises a test waveform.

7. The system of claim 1, wherein the transmission circuitry driver comprises current sensing circuitry.

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8. The system of claim 1, further comprising an analog system including:

- a digital to analog converter disposed between the digital system and an input of the transmission circuitry driver;
- a digital modulator disposed between the digital system and the digital to analog converter;
- a current multiplying impedance adaptive line driver coupled between the digital to analog converter and an output of the transmission circuitry driver; and
- an impedance adaptation sensor disposed between the current multiplying impedance adaptive line driver and the output of the transmission circuitry driver.

9. A method, comprising:

- producing a deterministic signal by a digital system;
- driving, through transmission circuitry, the deterministic signal onto a powerline in a powerline communication network with an unknown impedance load;
- measuring a quality of an output signal from the powerline;
- producing a first signal by the digital system;
- modifying a gain of the first signal based on the quality of the output signal; and
- driving the first signal onto the powerline with the modified gain.

10. The method of claim 9, wherein modifying the gain of the first signal further comprises changing a gain of the first signal in an analog system disposed between the digital system and an input of a driver that drives the deterministic signal and the first signal onto the powerline.

11. The method of claim 9, wherein modifying the gain of the first signal further comprises changing a gain of the first signal in a converter that converts between analog and digital.

12. The method of claim 9, wherein measuring the quality of the output signal from the powerline and modifying the gain of the first signal based on the quality of the output signal occurs until a desired performance of the first signal is achieved.

13. The method of claim 9, wherein measuring the quality of the output signal comprises measuring a distortion of the output signal.

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14. The method of claim 9, wherein measuring the quality of the output signal comprises measuring a voltage of the output signal.

15. The method of claim 9, wherein measuring the quality of the output signal comprises measuring a current of the output signal.

16. The method of claim 9, wherein the deterministic signal comprises a test waveform.

17. A system, comprising:

- a transmitter driver configured to drive a deterministic signal and a first signal onto a powerline in a powerline communication network, the powerline having an unknown impedance load thereon;
- a digital system coupled to an input of the transmitter driver and configured to produce the deterministic signal and the first signal;
- feedback circuitry configured to measure a quality of an output signal from the powerline based on the deterministic signal and to modify a gain of the first signal produced by the digital system based on the quality of the output signal; and

wherein the first signal, with modified gain, is driven by the transmitter driver onto the powerline.

18. The system of claim 17, wherein the transmitter driver includes an input and an output and the system further comprises feedback gain circuitry coupled between the output and the input.

19. The system of claim 17, wherein the transmitter driver includes an input and an output and wherein the feedback circuitry comprises a measurement system and load limiting logic, the measurement system being coupled between the output of the transmitter driver and the load limiting logic and wherein the measurement system is configured to measure the quality of the output signal.

20. The system of claim 19, further comprising an analog system including a digital to analog converter disposed between the digital system and the input of the transmitter driver.

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